Sub-10-nm-Diameter InGaAs Vertical Nanowire MOSFETs: Ni Versus Mo Contacts

Xin Zhao, *Member, IEEE*, Christopher Heidelberger, Eugene A. Fitzgerald, Wenjie Lu, *Student Member, IEEE*, Alon Vardi, *Member, IEEE*, and Jesús A. del Alamo, *Fellow, IEEE*

***Abstract*— Recently, sub-10-nm-diameter InGaAs vertical nanowire (VNW) MOSFETs have been demonstrated. The key to this achievement was the use of Ni for the top ohmic contact. In this paper, we present a detailed study of the impact of Ni and Mo contacts on the electrical characteristics of highly scaled InGaAs VNW MOSFETs. Sequential annealing experiments are presented that reveal the optimum temperature for each type of contact. A negative temperature dependence of the ON-resistance of 7-nm-diameter Ni-contacted devices suggests the existence of an energy barrier. We also observe an unexpected transconductance and drain-induced barrier loweirng (DIBL) dependence on transistor diameter in Ni-contacted devices as well as abnormal DIBL asymmetry to swapping source and drain. All these results can be explained by Ni diffusing down the nanowire during the contact annealing process, reducing the effective channel length, and creating a Schottky-barrier drain.**

***Index Terms*— Digital etch (DE), InGaAs, MOSFETs, nanowire (NW), reactive-ion etching (RIE), top–down, vertical channel.**

I. Introduction

FUTURE deeply scaled logic transistor technology can benefit from new channel materials including InGaAs [1], [2] as well as highly 3-D transistor structures, such as fin or nanowire (NW) geometries [3]. Recent circuit-level simulations have revealed that vertical NW (VNW) MOSFETs offer better performance, consume less power, and occupy the smaller area than horizontal NW MOSFETs [4]. This advantage is attributed to the relaxed gate length, spacer thickness, and contact length that the vertical geometry affords, as opposed to the very tight contacted-gate pitch constraints of horizontal devices.

Combining a high-mobility channel material, such as InGaAs, with a VNW transistor geometry is particularly interesting as the VNW geometry opens the door to heterojunction engineering in the transport direction. This new design freedom, not possible in all other lateral transistor configurations, potentially offers significant advantages, such as a reduction in gate-induced drain leakage [5]. In addition, the relaxed gate length scaling that the VNW architecture enables can alleviate the direct source-to-drain tunneling that is prominent in InGaAs MOSFETs with ultrascaled dimensions [6].

InGaAs VNW MOSFETs with impressive performance have been demonstrated by bottom–up [7]–[9] as well as top–down techniques [10]–[13]. In both approaches, contact to the top of the NW is a very problematic issue as a result of the tiny contact area that is available [13]. This represents a major challenge for NW diameter scaling below 10 nm, as demanded by the future ultrascaled logic applications [4].

Recently, by the use of Ni-alloyed contacts, the first InGaAs VNW MOSFETs with sub-10 nm diameter were realized [14]. In this first demonstration, several unexpected observations were made. The peak transconductance ($g_{m,\mathrm{pk}}$) was found to improve as the device diameter scales down to 7 nm, contrary to earlier observations [10]. Also, DIBL displayed an anomalous scaling behavior. A detailed study of these unique devices is valuable in our quest to identify directions for future device improvement.

In this paper, we study the key electrical figures of merit (FOMs) of sub-10-nm InGaAs VNW MOSFETs first presented in [14] and examine the role of the top contact in detail. Section II summarizes the device structure and process flow in greater detail, as compared to [14]. Section III discusses the effect of rapid thermal annealing (RTA) on device characteristics. The impacts of diameter scaling and device source/drain asymmetry are discussed in Section IV. Measurements at different temperatures and their analysis are presented in Section V. Section VI discusses the role of top contact in explaining the anomalous diameter scaling behavior of $g_{n,\mathrm{pk}}$ and DIBL in Ni-contacted devices.

II. Device Under Investigation

Fig. 1 shows the schematic cross section of the top–down InGaAs VNW MOSFETs studied in this paper [14]. Fig. 1 illustrates a device with a top Ni contact. Similar devices with top Mo contacts were also fabricated, as detailed in the following.

The starting heterostructure [14], also sketched in Fig. 1, consists of an 80-nm undoped $In_{0.53}Ga_{0.47}As$ channel sandwiched between two n^+ contact regions. The top contact

Manuscript received July 2, 2018; accepted July 17, 2018. Date of publication August 9, 2018; date of current version August 21, 2018. This work was supported in part by the NSF Center for Energy Efficient Electronics Science under Award 0959514, in part by Lam Research, and in part by SRC under Contract #2016-LM-2655. The review of this paper was arranged by Editor G. Meneghesso. *(Corresponding author: Xin Zhao.)*

X. Zhao, W. Lu, A. Vardi, J. A. del Alamo are with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: xinzhao@mit.edu).

C. Heidelberger and E. A. Fitzgerald are with the Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2018.2859202

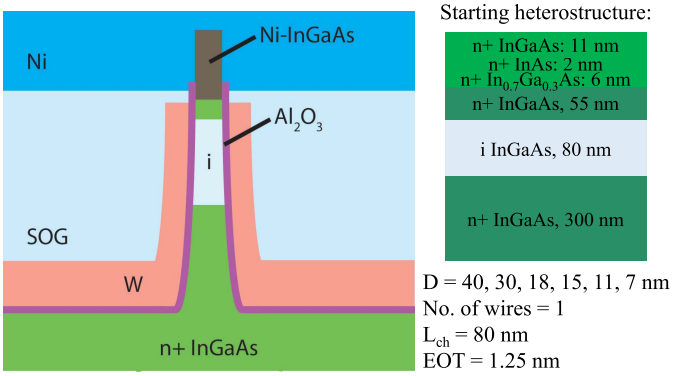


Fig. 1. Schematics of the device cross section, starting heterostructure, and device design parameters. In the heterostructure, the InGaAs composition is latticed matched to the InP substrate, unless indicated otherwise.

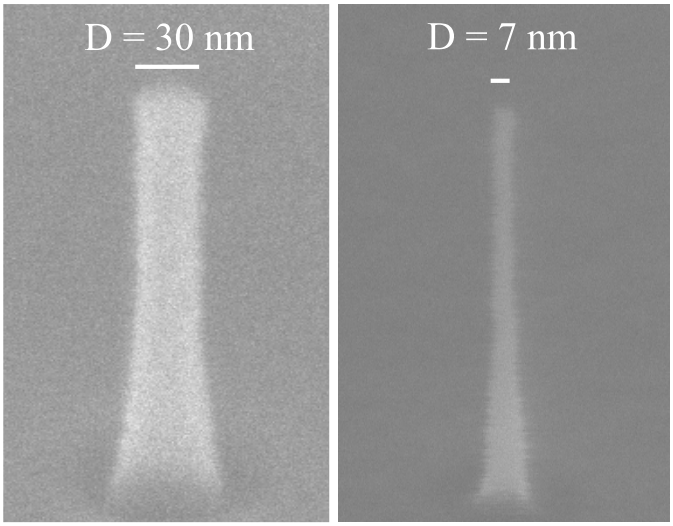


Fig. 2. D = 30 nm InGaAs NW right after RIE (left) reduced to D = 7 nm (right) after 10 cycles of DE with 10% H_2SO_4 in methanol.

region features a highly doped composite cap comprised, from top, 11-nm $In_{0.53}Ga_{0.47}As$/2-nm InAs/6-nm $In_{0.7}Ga_{0.3}As$ (n^+-doped with Te at a level of 7×10^{19} cm^{-3}) on the top of 55-nm $In_{0.53}Ga_{0.47}As$ (n^+-doped with Si at 2×10^{19} cm^{-3}). The bottom n^+ InGaAs is also doped with Si at 2×10^{19} cm^{-3}. This design was intended to reduce the contact resistance as InGaAs forms better ohmic contacts when the InAs composition is high [15], [16]. The top-most 11-nm $In_{0.53}Ga_{0.47}As$ layer was designed to be sacrificed during the process to reveal the underlying layers with a higher InAs composition. The 80-nm undoped InGaAs layer serves as the channel below which there is a 300-nm-thick n^+-layer that serves at the bottom contact. The entire heterostructure is grown by the metal–organic chemical vapor deposition on a semi-insulating InP substrate.

Device fabrication followed our previous work [9], [14] and featured a precision InGaAs dry etch technology to create ultrascaled, high aspect ratio nanopillars with a vertical and smooth sidewall [17].

To obtain sub-10-nm NWs with high yield, seven cycles of a newly developed alcohol-based digital etch (DE) [18] were carried out in 10% (volume concentration) H_2SO_4: methanol. An SEM image of an exemplary NW before and after DEs is shown in Fig. 2. Conventional water-based DE [19] results in NW destruction when attempting to cross below 10 nm in diameter (D) [18]. This is due to strong mechanical forces that arise from the high surface tension of the water-based acid used in the oxide removal step. Acids dissolved in alcohol feature a much lower surface tension and can enable remarkable scaling of NW diameter with high yield [18].

Immediately following the last cycle of DE, 2.5-nm Al_2O_3, as gate dielectric, is deposited on the sidewalls by atomic layer deposition (ALD). A 40-nm-thick W gate is then sputtered. This is immediately followed by a forming gas anneal step at 350 °C for 30 min to alleviate reactive-ion etching (RIE) damage [20] and improve the oxide/semiconductor interface. Two steps of planarization and etch back process using spin-on glass were then used to expose the NW tip for top contact formation while isolating the top contact metal from the gate metal [10]. The distance between the top edge of the gate and the bottom edge of the contact is 15 nm.

A critical challenge to obtain functional sub-10-nm VNW devices is contacting the tiny NW top. The use of Mo, which yields state-of-the-art contact resistance in planar transistors [21], becomes ineffective as the top contact in narrow fins and NWs because of the existence of a "dead zone" under the metal [21]. Even in the case of a Mo contact to a heavily doped InGaAs region, the outermost ~10-nm subsurface layer beneath the sidewall ends up being nonconducting. The origin of this problem is not fully understood but it appears to be due to both electrostatic sidewall depletion and mobility degradation [22].

In contrast with this, Ni has been shown to react with InGaAs at a moderate temperature and form a highly conducting NiInGaAs metallic phase that yields a low resistance contact to n^+-InGaAs [23]–[26]. In our process, the sample is split at this point and both Mo and Ni are separately sputtered as contact metal with a thickness of 30 nm. The conformity of both metals was confirmed through SEM on fin structures with the same dimensions as the NWs. Following this, and with the goal of improving the contact resistance, a 1-min final RTA step was performed. As detailed below, temperatures between 200 °C and 350 °C were investigated.

The finished transistors feature a single NW with a channel length of 80 nm (the thickness of the intrinsic InGaAs layer, as shown in Fig. 1), D = 7, 11, 15, 18, 30 or 40, and 2.5 nm Al_2O_3 gate oxide (equivalent oxide thickness of 1.25 nm).

Finished devices were electrically characterized by measuring output, transfer, and subthreshold characteristics at different temperatures. In this paper, we mostly focus on six key electrical FOMs: peak transconductance $g_{m,\mathrm{pk}}$ at V_{ds} = 0.5 V, ON-resistance R_{ON} extracted at V_{gs} = 1 V and small V_{ds} (0.05 V), ON-current I_{ON} defined at I_{OFF} = 100 nA/μm and V_{dd} = 0.5 V, minimum subthreshold swing at V_{ds} = 0.05 V S_{lin}, threshold voltage $V_{t,\mathrm{lin}}$ extracted at I_d = 1 μA/μm and V_{ds} = 0.05 V, and DIBL defined as the ratio of the threshold voltage difference at V_{ds} = 0.05 V and V_{ds} = 0.5 V divided by the drain voltage difference (450 mV).

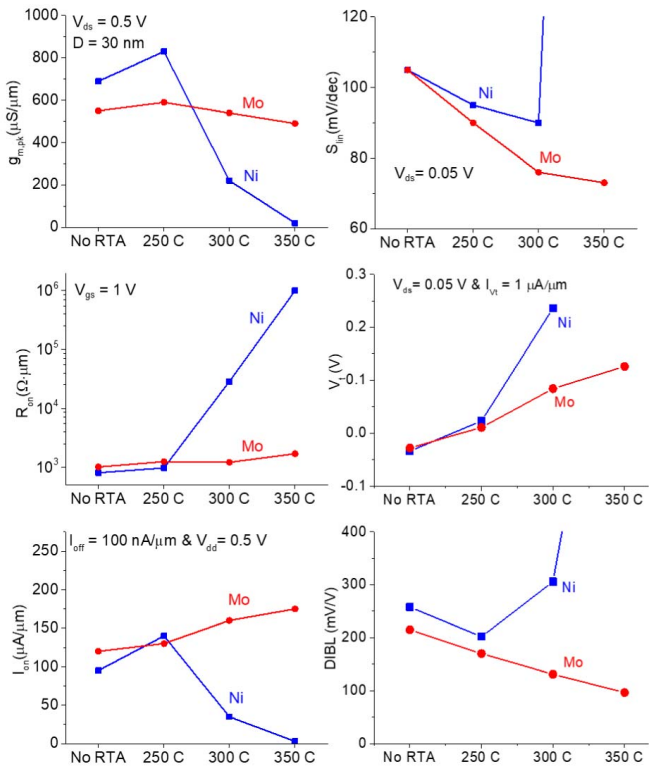


Fig. 3. Evolution of key FOMs with RTA annealing temperature on Mo- and Ni-contacted transistors with $D = 30$ nm diameter in sequential annealing experiments. The bottom contact serves as the source.

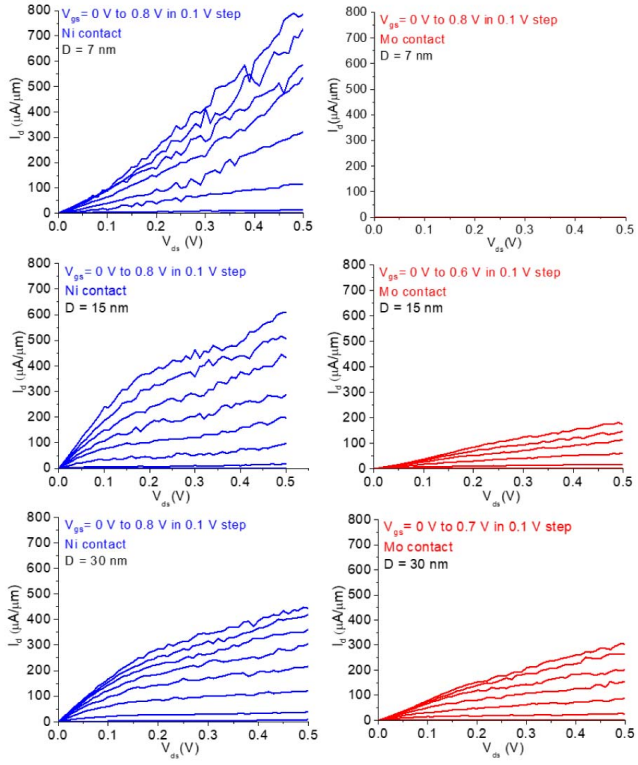


Fig. 4. Representative output characteristics of Ni- and Mo-contacted devices after annealing under optimal conditions. Devices with D = 7, 15, and 30 nm are shown. All measurements performed with the source at the bottom.

III. Impact of Rapid Thermal Annealing Temperature

To better understand the effect of thermal annealing and find the optimal annealing temperature (T), sequential RTA in N_2 ambient was carried out at 250 °C, 300 °C, and 350 °C for both Ni and Mo contacts. The evolution of key device FOMs for $D = 30$ nm devices as a function of annealing temperature is summarized in Fig. 3. Each data point represents the mean value of three devices. In these results, the bottom electrode was used as the source.

Mo devices (red data) show relatively small changes with RTA, as expected from a refractory metal. While $g_{m,\mathrm{pk}}$ and R_{ON} remain rather flat until 350 °C, S_{lin} drops with increasing T as annealing improves the intrinsic oxide–semiconductor interface and reduces the interface trap density (D_{it}) inside the bandgap [27]. This also results in a continuous enhancement of I_{ON} up to 350 °C. Positive V_t shift is observed after annealing, potentially due to the reduction of positive fixed charge in ALD Al_2O_3 [27]. Interestingly, DIBL also drops after RTA at higher T, suggesting the role of traps.

RTA is found to have a much more pronounced effect in Ni-contacted devices (blue data). Annealing at 250 °C enhances $g_{m,\mathrm{pk}}$. We attribute this to an improvement in the top contact. However, the Ni contacts deteriorate rapidly after annealing at 300 °C. As a result, I_{ON} first increases with annealing but eventually crashes at temperatures above 250 °C. Up to this temperature, S_{lin} and DIBL also improve. A more detailed explanation of all these changes is presented in Section VI.

These sequential annealing experiments were carried out on small pieces cutoff from the main samples. Based on them plus other single-temperature studies not discussed here, an annealing temperature of 300 °C for 1 min in N_2 was selected for the main batch of Mo devices for all diameters. Regarding the Ni devices, since the starting temperature for the sequential annealing measurements shown in Fig. 3 was 250 °C, and this was found to be the optimum annealing temperature, the device sample was first annealed at 200 °C under forming gas. The obtained results were better than at 250 °C in the test sample and no further annealing was performed.

IV. Diameter Scaling and Source/Drain Asymmetry

Representative output characteristics of Ni-contacted (blue) and Mo-contacted (red) devices at $D = 7$, 15, and 30 nm are shown in Fig. 4 on identical scales. Generally, the Ni-contacted devices show significantly more current than the Mo transistors. The smallest diameter for functional devices with Mo contacts was found to be 15 nm, while many working $D = 7$ nm Ni-contacted transistors were obtained. Good output current saturation is obtained in Ni devices with $D = 30$ nm. The $D = 7$ nm devices, however, show diode-like turn-ON. This can be attributed to the top contact, as discussed in Section VI.

Fig. 5 summarizes the key FOMs as a function of diameter for Ni and Mo devices after the optimizing final annealing

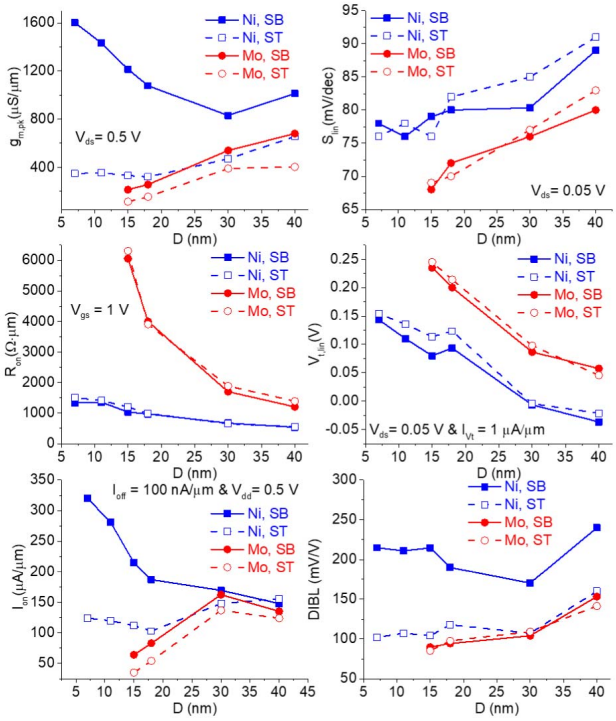


Fig. 5. Impact of diameter scaling and source/drain asymmetry in key FOMs for Ni- and Mo-contacted transistors annealed under optimum conditions.

(each data point represents the average of three transistors). Fig. 5 also shows the impact of swapping source and drain contacts [12]. In the normal configuration, the source is at the bottom as SB. This generally yields the best all-around performance. We denote the inverse configuration in which the source is at the top as ST.

Classical diameter scaling behavior is observed in the electrostatics metrics of Mo-contacted devices (red). The subthreshold swing and DIBL improve as D is reduced and V_t shifts positive. As expected, R_{ON} increases as D is scaled down and consequently $g_{m,pk}$ drops. I_{ON} reaches a peak at $D = 30$ nm due to the tradeoff between electrostatics and contact resistance. Below $D = 15$ nm, the transistors are nonfunctional due to an open top contact. This result supports the existence of a "dead zone" under the Mo contact [22].

When it comes to source/drain swapping, as in [12], Fig. 5 shows that the Mo-contacted devices are very symmetric in their electrostatic behavior. As in [12], we attribute this to our dry etch technology that produces a uniform NW cross section toward the top where the intrinsic device is located. This can be seen in Fig. 2. The somehow lower $g_{m,pk}$ and I_{ON} in the ST configuration reflects the higher contact resistance associated with the very small top contact.

For Ni devices (blue) in the SB configuration, V_t shifts positive and S_{lin} improves as D shrinks. This is expected from classic electrostatic scaling. In contrast, DIBL first drops and then, unexpectedly, increases. This matches the worsening current saturation in the output characteristics in devices with the smaller diameter that is shown in Fig. 4. We come back to this below. DIBL and S_{lin} are worse for Ni-contacted devices

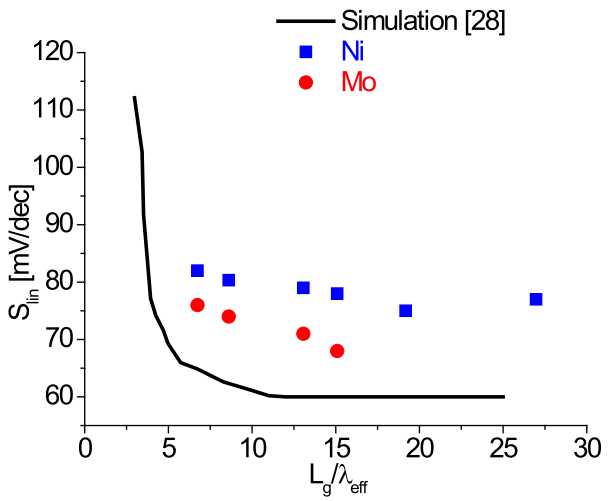


Fig. 6. S_{lin} versus L_g/λ_{eff} for both Ni- and Mo-contacted devices measured with the source at the bottom. Black line: ideal electrostatic simulation [28]. Data points correspond to experimental results reported in this paper.

as compared with Mo. This is because Mo allows a higher annealing temperature that further improves the intrinsic MOS interface.

The most interesting behavior of the Ni-contacted devices in the SB configuration is that they show a dramatic improvement in $g_{m,pk}$ despite a slightly rising R_{ON} as D scales down. This abnormal $g_{m,pk}$ scaling is also attributed to the top contact and is discussed in detail in Section VI. R_{ON} for Ni devices is much smaller and increases much more slowly as D shrinks, demonstrating the advantage of Ni-alloyed contacts for extremely scaled VNW transistors. As a consequence of the improving subthreshold swing and transconductance, I_{ON} increases in a pronounced manner down to $D = 7$ nm.

Similar to Mo, $g_{m,pk}$ and I_{ON} in Ni devices are much lower when the top electrode is used as source as a result of the high top contact resistance. As in Mo devices, R_{ON}, S_{lin}, and V_t do not exhibit much difference in the ST and SB configurations. This is again testament to the excellent diameter uniformity at the top of the NW. In contrast, DIBL shows considerable S/D asymmetry in Ni-contacted devices at all diameters. The ST configuration yields significantly better DIBL than when the source is at the bottom. The origin of this is not clear and discussed further in Section VI.

To gain further insight into the device electrostatics and D_{it} levels, Fig. 6 shows S_{lin} of Ni- and Mo-contacted VNW MOSFETs as a function ofL_g/λ_{eff}. L_g is the gate length, and λ_{eff} is the natural electrostatic length which is a measure of how far into the channel the drain impacts the channel potential [28]. To the first order, λ_{eff} is given by

$$\lambda_{eff} = \sqrt{\frac{\pi \epsilon_s D^2}{4C_{ox}} + \frac{D^2}{16}} \tag{1}$$

where ϵ_s is the dielectric constant of the channel material, and C_{ox} is the gate oxide capacitance

$$\frac{1}{C_{ox}} = \frac{\ln\left(1 + \frac{2t_{ox}}{D}\right)}{2\pi\epsilon_{ox}}. \tag{2}$$

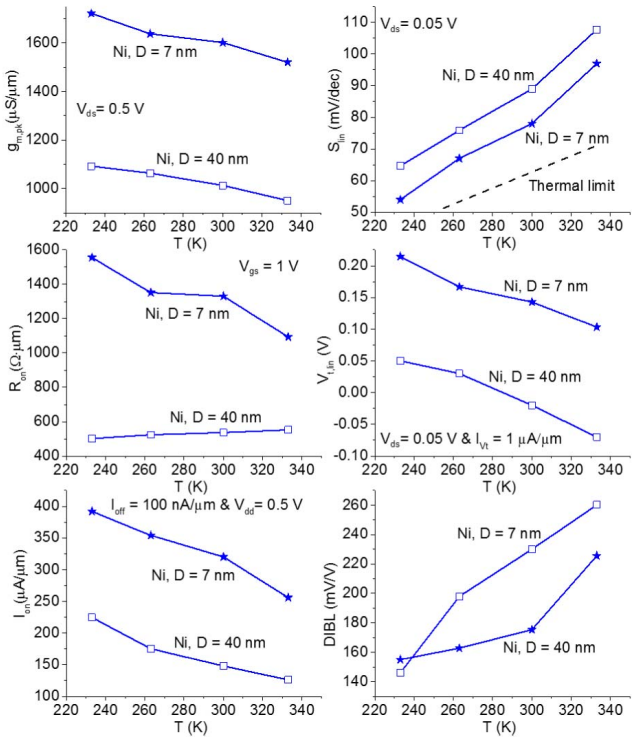


Fig. 7. Temperature dependence of key FOMs for Ni-contacted devices of two different diameters. In all the cases, the source is at the bottom.

Here, t_{ox} and ϵ_{ox} are the thickness and dielectric constant of the oxide. The black line in Fig. 6 is the ideal relationship obtained from electrostatic simulations [28]. Multiple reports from the literature, including some of our own [21], show S_{lin} substantially worse than the ideal value. This is attributed to poor gate efficiency η due to oxide/semiconductor interface traps [27]. Including this, S_{lin} becomes

$$S_{lin} = S_0 \times \eta \approx S_0 \times \left(1 + \frac{q\pi D D_{it}}{C_{ox}}\right) \tag{3}$$

where S_0 is the ideal subthreshold swing shown by the black line in Fig. 6. Based on (3), we estimate D_{it} to be around 6 and 4×10^{12} eV$^{-1}\cdot$cm^{-2}, for Ni and Mo devices, respectively. The higher annealing temperature used for the Mo devices results in a lower D_{it} level.

V. Temperature Dependence

To gain further insight into the dominant physics, both Ni and Mo transistors were characterized at various temperatures from 230–330 K. Key FOMs for Ni devices with $D = 7$ and 40 nm and SB configuration are shown in Fig. 7. For the $D = 40$ nm device, S_{lin} drops as T decreases, as expected. DIBL rapidly improves at lower T confirming again the role of traps. Slightly lower R_{ON} is also obtained at lower temperatures, potentially due to a decreased series resistance of the n$^+$ contact region as a result of small increase in mobility. $g_{m,pk}$ improves as the temperature is reduced. A number of factors, including higher mobility and less charge trapping at lower T, are likely to contribute to this. As a result of higher transconductance and lower S_{lin} at lower T,

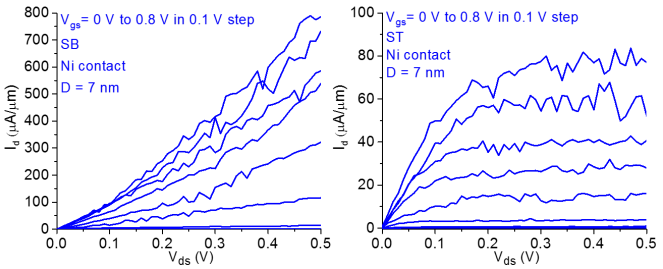


Fig. 8. Output characteristics measured with SB (left) versus ST (right) of a representative $D = 7$ nm Ni-contacted transistor.

I_{ON} is also enhanced at low temperatures. Similar temperature dependencies have been observed in transistors with Mo contacts of all diameters (data not shown).

Ni-contacted devices with $D = 7$ nm show a similar behavior as the wider devices with one important exception, i.e., R_{ON} exhibits a strong negative temperature dependence. This is a key observation that we attribute to the top contact, as discussed in Section VI.

VI. Role of the Top Contact

This first realization of sub-10-nm-diameter InGaAs VNW MOSFETs has yielded a number of surprises in the narrow D regime that Ni contacts have made possible. A rapidly improving $g_{m,pk}$ as D scales down, and a negative temperature dependence of R_{ON} are unexpected. The details of the top Ni contact provide an explanation to these phenomena.

It is well known that when Ni reacts with InGaAs at a moderate temperature, a highly conducting NiInGaAs metallic phase is formed [23]–[26], [29], [30]. It has also been observed that during thermal annealing of Ni-contacted InGaAs FinFETs, Ni diffuses along the fins as it forms NiInGaAs [31]. A higher rate of diffusion is observed in narrower fins because the diffusion is surface limited and narrower fins have a higher surface-to-volume ratio.

From these observations, it is reasonable to expect that in our devices, Ni diffuses further down the NW the narrower its diameter. For our annealing conditions, when $D < 20$ nm, Ni might diffuse through the entire n$^+$-doped layer stack and reach the undoped channel region. This would have two consequences. First, the effective electrical channel length becomes shorter, yielding an increasing transconductance, as shown in Fig. 5. In addition, the NiInGaAs comes now in direct contact with undoped InGaAs. Rather than an ohmic contact, this could result in a Schottky barrier [32]. In this instance, R_{ON} should show a negative temperature dependence, as observed in Fig. 7.

Confirmation of this hypothesis comes from a comparison of the output characteristics of a $D = 7$ nm Ni device measured in the SB and ST configuration, as shown in Fig. 8. (The left characteristics are the same as those in the left corner of Fig. 4.) As discussed earlier, when the source is at the bottom and the device is biased in the saturation regime, the Schottky diode at the drain is forward biased and the output characteristics show Schottky-like behavior [Fig. 8 (left)]. With the source at the top, the transistor exhibits

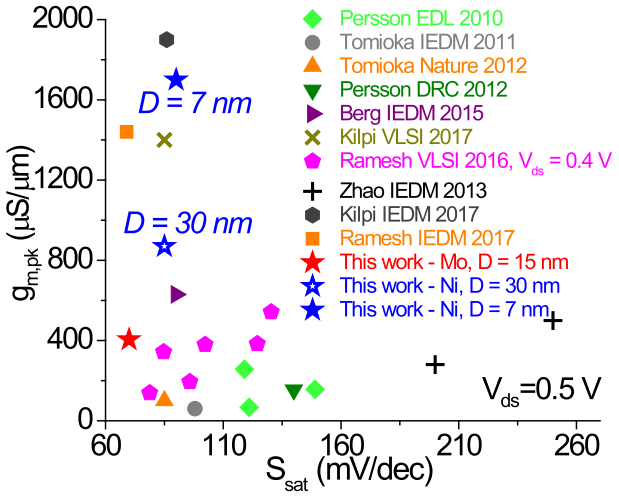


Fig. 9. Benchmark: $g_{m,\mathrm{pk}}$ versus minimum S_{sat} at $V_{\mathrm{ds}} = 0.5$ V for InGaAs-based VNW MOSFETs.

excellent current saturation but with much lower current [Fig. 8 (right)]. In this configuration, the transistor behaves like a metal-source Schottky-barrier MOSFET with relatively high source resistance but good drain current saturation.

Fig. 5 shows that DIBL exhibits considerable S/D asymmetry in Ni devices of all diameters and is higher when the top electrode behaves as the drain. This asymmetry can potentially be caused by a diameter change in the semiconductor beneath the NiInGaAs region because of the strain introduced by NiInGaAs formation [31]. Zhao *et al.* [12] show that the diameter nonuniformity results in DIBL asymmetry. The band structure of InGaAs can also change because of the strain and might lead to DIBL asymmetry. In addition, charge trapping can potentially play a role. Further detailed characterization of the NiInGaAs phase in the very small VNW via TEM, or other techniques is needed to verify our hypothesis.

Fig. 9 shows the benchmarks transport and electrostatics metrics in recently published InGaAs VNW MOSFETs by plotting $g_{m,\mathrm{pk}}$ versus minimum S_{sat}, both at $V_{\mathrm{ds}} = 0.5$ V. This graph captures the tradeoff that often exists between transport and electrostatics in MOSFETs. Our $D = 7$ nm device with Ni contact shows a combination of high transconductance and good subthreshold swing, highlighting the potential of the top–down VNW approach.

It is of interest to compare our best $D = 30$ nm Ni-contacted device (plotted in Fig. 9) with the device that exhibits the highest $g_{m,\mathrm{pk}}$ in Fig. 9 that has a $D = 27$ nm [9]. R_{ON} in our device is around 650 $\Omega \cdot \mu$m while that of [9] reaches 450 $\Omega \cdot \mu$m. This excellent result might be due to the longer top contact region and leads to higher $g_{m,\mathrm{pk}}$. Our device demonstrates comparable S_{sat} of 85 mV/dec (versus 86 mV/dec in [9]). With $D = 15$ nm, our Mo-contacted MOSFET exhibits one of the lowest S_{sat} of 70 mV/dec (63 mV/dec reported for $D = 30$ nm in [13]).

Indeed, the top contact remains a key challenge for III–V VNW technology, especially at the scaled dimensions required for future nodes. Mo does not yield working contacts and Ni contacts are unlikely to survive the standard back-end-of-line process due to significant diffusion at even relatively low temperatures. Significant efforts are, therefore, required in order to develop a suitable contact technology that minimizes contact resistance while ensuring thermal stability. Refractory metals including Mo will likely require a mushroom contact [9], or InGaAs with high InAs composition [15], [16]. Alloyed contacts need careful optimization of the amount of metal to prevent excess diffusion.

VII. Conclusion

Extensive characterization was carried out of InGaAs VNW MOSFETs with both Ni and Mo contacts down to the sub-10 nm in diameter. The use of Ni as the top contact has been the key to achieve working transistors in this diameter regime. Temperature dependence of ON-resistance, high transconductance, and high DIBL in Ni-contacted devices with narrow diameter suggests that Ni diffuses along the NW and reduces the effective channel length.

Acknowledgment

Device fabrication was carried out at the Microsystems Technology Laboratories and Electron Beam Lithography Laboratory of MIT, Cambridge, MA, USA.

References

[1] J. A. del Alamo, "Nanometer-scale electronics with III–V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, Nov. 2011.
[2] H. Riel, L.-E. Wernersson, M. Hong, and J. A. del Alamo, "III–V compound semiconductor transistors-from planar to nanowire structures," *MRS Bull.*, vol. 39, no. 08, pp. 668–677, Aug. 2014.
[3] K. J. Kuhn, "Considerations for ultimate CMOS scaling," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, Jul. 2012.
[4] D. Yakimets *et al.*, "Vertical GAAFETs for the ultimate CMOS scaling," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1433–1439, May 2015.
[5] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Physics and mitigation of excess off-state current in InGaAs quantum-well MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1448–1455, May 2015.
[6] V. Moroz, J. Huang, and R. Arghavani, "Transistor design for 5 nm and beyond: Slowing down electrons to speed up transistors," in *ISQED Tech. Dig.*, Mar. 2016, pp. 278–283.
[7] C. Thelander, L. E. Fröberg, C. Rehnstedt, L. Samuelson, and L.-E. Wernersson, "Vertical enhancement-mode InAs nanowire field-effect transistor with 50-nm wrap gate," *IEEE Electron Device Lett.*, vol. 29, no. 3, pp. 206–208, Mar. 2008.
[8] K. Tomioka, M. Yoshimura, and T. Fukui, "A III–V nanowire channel on silicon for high-performance vertical transistors," *Nature*, vol. 488, no. 7410, pp. 189–192, Aug. 2012.
[9] O.-P. Kilpi, J. Svensson, and L.-E. Wernersson, "Sub-100-nm gate-length scaling of vertical InAs/InGaAs nanowire MOSFETs on Si," in *IEDM Tech. Dig.*, Dec. 2017, pp. 417–420.
[10] X. Zhao, J. Lin, C. Heidelberger, E. A. Fitzgerald, and J. A. del Alamo, "Vertical nanowire InGaAs MOSFETs fabricated by a top-down approach," in *IEDM Tech. Dig.*, Dec. 2013, pp. 695–698.
[11] S. Ramesh *et al.*, "Top-down InGaAs nanowire and fin vertical FETs with record performance," in *VLSI Tech. Dig.*, Jun. 2016, pp. 164–165.
[12] X. Zhao, J. Lin, C. Heidelberger, E. A. Fitzgerald, and J. A. del Alamo, "Source/drain asymmetry in InGaAs vertical nanowire MOSFETs," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2161–2165, May 2017.
[13] S. Ramesh *et al.*, "Record performance top-down $In_{0.53}Ga_{0.47}As$ vertical nanowire FETs and vertical nanosheets," in *IEDM Tech. Dig.*, Dec. 2017, pp. 409–412.
[14] X. Zhao, C. Heidelberger, E. A. Fitzgerald, W. Lu, A. Vardi, and J. A. del Alamo, "Sub-10 nm diameter InGaAs vertical nanowire MOSFETs," in *IEDM Tech. Dig.*, Dec. 2017, pp. 413–416.

[15] T. Nittono, H. Ito, O. Nakajima, and T. Ishibashi, "Non-alloyed ohmic contacts to n-GaAs using compositionally graded $In_xGa_{1-x}As$ layers," *Jpn. J. Appl. Phys.*, vol. 27, no. 9, pp. 1718–1722, Jul. 1988.
[16] S. Kim *et al.*, "High-performance InAs-on-insulator n-MOSFETs with Ni-InGaAs S/D realized by contact resistance reduction technology," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3342–3350, Oct. 2013.
[17] X. Zhao and J. A. del Alamo, "Nanometer-scale vertical-sidewall reactive ion etching of InGaAs for 3-D III–V MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 521–523, May 2014.
[18] W. Lu, X. Zhao, D. Choi, S. El Kazzi, and J. A. del Alamo, "Alcohol-based digital etch for III–V vertical nanowires with sub-10 nm diameter," *IEEE Electron Device Lett.*, vol. 38, no. 5, pp. 548–551, May 2017.
[19] J. Lin, X. Zhao, D. A. Antoniadis, and J. A. del Alamo, "A novel digital etch technique for deeply scaled III–V MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 440–442, Apr. 2014.
[20] J. Lin, T.-W. Kim, D. A. Antoniadis, and J. A. del Alamo, "A self-aligned InGaAs quantum-well metal–oxide–semiconductor field-effect transistor fabricated through a lift-off-free front-end process," *Appl. Phys. Express*, vol. 5, no. 6, p. 064002, May 2012.
[21] J. A. del Alamo, D. A. Antoniadis, J. Lin, W. Lu, A. Vardi, and X. Zhao, "Nanometer-scale III–V MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 4, no. 5, pp. 205–214, Sep. 2016.
[22] A. Vardi and J. A. del Alamo, "Fin-width scaling of highly-doped InGaAs fins," in *Proc. Compound Semiconductor Week*, Cambridge, MA, USA, May/Jun. 2018.
[23] S.-H. Kim *et al.*, "Self-aligned metal source/drain $In_xGa_{1-x}As$ n-MOSFETs using Ni-InGaAs alloy," in *IEDM Tech. Dig.*, Dec. 2010, pp. 596–599.
[24] X. Zhang, Ivana, H. X. Guo, X. Gong, Q. Zhou, and Y.-C. Yeo, "A self-aligned Ni-InGaAs contact technology for InGaAs channel n-MOSFETs," *J. Electrochem. Soc.*, vol. 159, no. 5, pp. 511–515, Mar. 2012. [Online]. Available: http://jes.ecsdl.org/content/159/5/H511.short
[25] M. L. Huang *et al.*, "High performance $In_{0.53}Ga_{0.47}As$ FinFETs fabricated on 300 mm Si substrate," in *VLSI Tech. Dig.*, Jun. 2016, pp. 16–17.
[26] L. Czornomaz *et al.*, "CMOS compatible self-aligned S/D regions for implant-free InGaAs MOSFETs," *Solid-State Electron.*, vol. 74, pp. 71–76, Aug. 2012.
[27] M. Si *et al.*, "Effects of forming gas anneal on ultrathin InGaAs nanowire metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 102, no. 9, p. 093505, 2013.
[28] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's," *IEEE Electron Device Lett.*, vol. 18, no. 2, pp. 74–76, Feb. 1997.
[29] R. Oxland *et al.*, "An ultralow-resistance ultrashallow metallic source/drain contact scheme for III–V NMOS," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 501–503, Feb. 2012.
[30] R. J. W. Hill *et al.*, "Self-aligned III–V MOSFETs heterointegrated on a 200 mm Si substrate using an industry standard process flow," in *IEDM Tech. Dig.*, Dec. 2010, pp. 130–133.
[31] R. Chen and S. A. Dayeh, "Size and orientation effects on the kinetics and structure of nickelide contacts to InGaAs fin structures," *Nano Lett.*, vol. 15, no. 6, pp. 3770–3779, Apr. 2015.
[32] S. Mehari, A. Gavrilov, S. Cohen, P. Shekhter, M. Eizenberg, and D. Ritter, "Measurement of the Schottky barrier height between Ni-InGaAs alloy and $In_{0.53}Ga_{0.47}As$," *Appl. Phys. Lett.*, vol. 101, no. 7, p. 072103, Aug. 2012.

Xin Zhao (M'13) received the B.S. degree in physics from Peking University, Beijing, China, in 2010, and the M.S. and Ph.D. degrees in materials science and engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2012 and 2017, respectively.

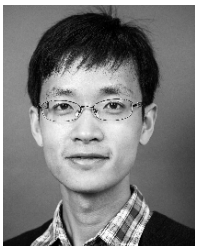
He has been holding the post-doctoral position at the Massachusetts Institute of Technology since 2017. His current research interests include III-V vertical nanowire transistor technologies for ultra-low power applications.

Christopher Heidelberger received the B.S. degree in materials science and engineering from Cornell University, Ithaca, NY, USA, in 2012. He is currently pursuing the Ph.D. degree with the Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, MA, USA.

His current research interests include III-V epitaxial growth, characterization of epitaxial films, and monolithic integration of III-V semiconductors on Si substrates for electronic and photonic applications.

Eugene A. Fitzgerald received the B.S. degree in materials science and engineering from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 1985, and the Ph.D. in materials science and engineering from Cornell University, Ithaca, NY, USA, in 1989.

He is currently the Merton C. Flemings–Singapore MIT Alliance Professor of materials engineering with MIT.



Wenjie Lu (S'14) received the M.S. degree from the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, USA, where he is currently pursuing the Ph.D. under the supervision of Prof. J. A. del Alamo.

His current research interests include the design and fabrication of nano-electronic devices for future logic and analog applications.

Alon Vardi (M'13) received the B.S. degree in electrical engineering from the University of Ariel, Ariel, Israel, in 2002, and the M.S. and Ph.D. degrees in electrical engineering from Technion–Israel Institute of Technology, Haifa, Israel, in 2006 and 2010, respectively.

He has been with the Massachusetts Institute of Technology, Cambridge, MA, USA, since 2013, where he is currently a Research Scientist with the Microsystems Technology Laboratories.

Jesús A. del Alamo (M'78–F'06) received the B.S. degree in telecommunications engineering from the Polytechnic University of Madrid, Madrid, Spain, in 1980, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1983 and 1985, respectively.

Since 1988, he has been with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, USA.